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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,603	06/27/2003	Paul Savage	70021171-1	2258

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AGILENT TECHNOLOGIES, INC.
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Intellectual Property Administration
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EXAMINER

DOAN, NGHIA M

ART UNIT PAPER NUMBER

2825

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/608,603

Applicant(s)

SAVAGE, PAUL

Examiner

Nghia M. Doan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 June 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 11-15 is/are rejected.
- 7) ☒ Claim(s) 7-10 and 16-19 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06/27/2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Responsive to communication application 10/608,603 filed on 06/27/2003, claims 1-19 are pending.

Claim Objections

2. Claims 2-3, 5-12, and 14-19 are objected to because of the following informalities:

As claims 2-3 and 5-12, the term "A method" changes to – the method--.

As claims 14-19, the term "A computer" changes to – the computer --

As claims 9 and 18 recite the limitation "a second logical AND " in page 14 line 5 and page 16 line 15. These claims depend on claims 4 and 13, respectively, while claims 4 and 13 are not including limitation that " a first logical AND ". Since claims 10 and 19 depend directly or indirectly on claims 9 and 18, they contain the limitation of those claims and therefore are also objected.

Examiner suggests that claims 9 and 18 depend on claim 7 and 16 as further limitations.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Schzukin (US 6,442,747).**

5. **With respect to claim 1**, Schzukin discloses a method of creating a logical device performing polynomial division (abstract), comprising:

(a) using a hardware description language to build code directly describing synthesizable logic for performing the polynomial division (fig. 2, step 36 and col. 2, ll. 7-11); and

(b) implementing the logic on a target device (col. 3, ll. 34-36 and ll. 49-51), wherein the code receives as inputs a parameter identifying a polynomial and a parameter identifying a number of data bits for which the polynomial division is performed (fig. 1, col. 3, ll. 42-53 and col. 2, ll. 36-52).

6. **With respect to claim 2**, Schzukin discloses the method according to claim 1 wherein the logical device is used in a cyclic redundancy checker (col. 1, ll. 18-22 -- cyclic redundancy code is a detector (checker) for checking error and may performing calculated to reduce number of gate in a circuit--)

7. **With respect to claim 3**, Schzukin discloses the method according to claim 1 wherein the target device includes a suitable logic device (complexity circuit) on which the logic may be implemented (col. 2, ll. 9-11).

8. **Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Gallezot et al (Gallezot) (US 2002/0144208).**

9. **With respect to claim 1**, Gallezot discloses a method of creating a logical device performing polynomial division (abstract), comprising:

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(a) using a hardware description language to build code directly describing synthesizable logic for performing the polynomial division (pg. 5, ¶71); and

(b) implementing the logic on a target device (FPGA) (pg. 5, ¶71), wherein the code receives as inputs a parameter identifying a polynomial and a parameter identifying a number of data bits for which the polynomial division is performed (fig. 10, pg. 2, ¶26).

10. **With respect to claim 2**, Gallezot discloses the method according to claim 1 wherein the logical device is used in a cyclic redundancy checker (pg. 1, ¶9)

11. **With respect to claim 3**, Gallezot discloses the method according to claim 1 wherein the target device includes FPGA (fig. 15, pg. 5, ¶71).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. **Claims 4-6, and 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallezot et al (Gallezot) (US 2002/0144208) in view of Schzukin (US 6,442,747).**

14. **With respect to claims 4 and 13**, Gallezot discloses a method and computer product of creating a logical device performing polynomial division for a given n-degree polynomial including calculating a next n-term remainder for a data unit having d terms (pg. 1, ¶9), the method and computer product using a high level description language

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directly describing synthesizable logic for performing the polynomial division, which is application for FPGA and any form of Programmable Logic Device (PLD) (pg. 5, ¶71). The polynomial division using the logic of XOR for synthesizing of next remainder on the subset of data terms for a preceding data unit (fig. 5, and pg. 3, ¶41 and pg. 5, ¶69).

Gallezot also discloses the method of calculating the Most and Last Significant Bits (MSB and LSB) of the data string, but Gallezot does not explicitly teach extracting data for calculating each of the next remainder term.

Schzukin does teach method of implementation CRC polynomial division with VHDL coding (fig. 2, step 36 and Listing 4 such as cols. 17, 19, and 21) for performing calculated remainder term by treating the data as coefficients of polynomial division for calculating each of the next remainder term (at least suggest at, col. 2, ll. 39-52; fig. 2, steps 24-30 and the description).

It would have been obvious to person of ordinary skill in the art would combines Schzukin and Gallezot references for generating high level circuit description language code representing a CRC generator circuit to implement a generator polynomial associated with generating remainder for optimizing code VHDL from 9 bits generator polynomial (Gallezot, pg. 3, ¶32) to 10 bits CRC generator polynomial using 32 data bits (Schzukin, Listing 4, col. 16, 17, 19, and 21). The optimized VHDL code (program) is eliminating a duplicate entries based on logic XOR operation and also reduce time delay, faster counting cell, and running time for the synthesizer.

15. **With respect to claims 5 and 14**, Schzukin discloses the limitations according to claims 4 and 13, respectively, wherein the logical XOR operation includes a pipelined

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XOR operation with a pre-definable number of pipeline stages, the pipelined XOR operation operating on the subset of data terms (Schzukin, fig. 1, and col.3, ll. 41-63).

16. **With respect to claims 6 and 15**, Schzukin discloses the limitations according to claims 5 and 14, respectively, wherein the number of pipeline stages is greater than or equal to 1(Schzukin, fig. 1, and col.3, ll. 41-63).

17. **With respect to claim 11**, Gallezot discloses the method according to claim 1 wherein the logical device is used in a cyclic redundancy checker (Gallezot, pg. 1, ¶9)

18. **With respect to claim 12**, Gallezot discloses the method according to claim 1 wherein the target device includes FPGA (Gallezot, fig. 15, pg. 5, ¶71).

Allowable Subject Matter

19. Claims 7-10 and 16-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

20. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach or suggest the following:

As per claims 7, 8, 16, and 17 that “ first logical AND gate operation eliminates data terms not required for calculating the next remainder”.

As per claims 9, 10, 18, and 19 that “performing a second logical AND on the identified remainder terms with the remainder terms calculated for the preceding data unit”.

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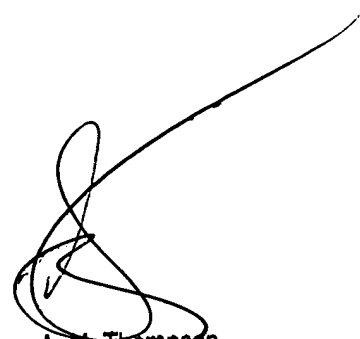
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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